SFAL

SEMICONDUCTOR FUTURE ACCELERATOR LAB FOUNDATION

Future Semisphere

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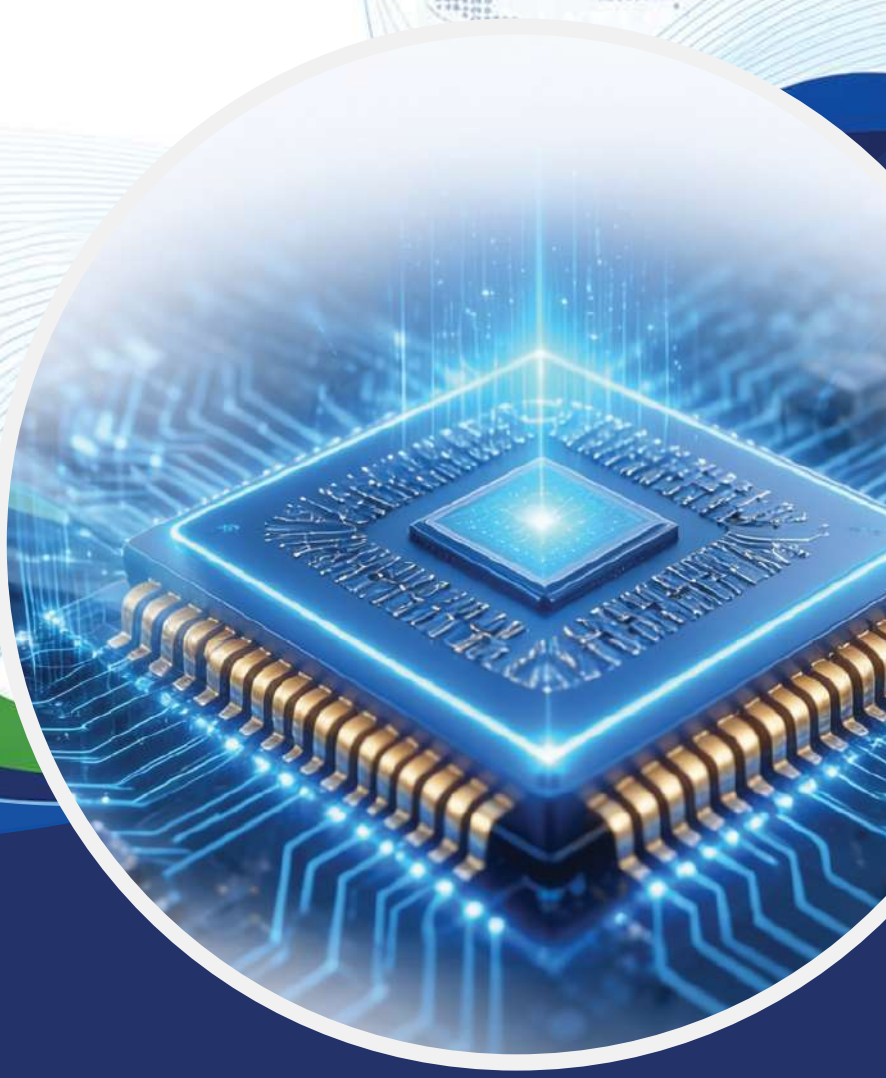

Technology | Investment | Supply Chain | Policy | Innovation

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INVESTMENT & MARKET

Design Wins & Custom Silicon · M&A and Consortia

OpenAI's Jalapeño and Qualcomm's Dragonfly: the buyers are becoming the chipmakers

The AI buyers are moving into silicon design, and two announcements in the same week showed how far. OpenAI and Broadcom unveiled Jalapeño, OpenAI's first custom inference processor, a reticle-sized ASIC built on a 3nm process and purpose-built for large-language-model serving rather than training. Broadcom handled the silicon and networking; Celestica handled rack assembly.

Qualcomm, meanwhile, laid out a full data-centre roadmap at its Investor Day: the Dragonfly C1000 CPU, the AI300 inference accelerator and a new near-memory High Bandwidth Compute (HBC) architecture that stacks compute beneath LPDDR to sidestep costly HBM and interposers. It claims six-times-higher bandwidth-per-watt than HBM and won a multi-generation commitment from Meta for Dragonfly CPUs, plus Microsoft Azure as an HBC adopter. First HBC silicon (AI250) is due to sample in mid-2027.

Both moves aim squarely at inference economics and the memory wall, and both chip away at the incumbent GPU model. The message for the industry is that the largest AI operators now treat custom silicon as core infrastructure, not an experiment.

What This Means For You

For Startups

IP and design-services teams should note the premium on inference-specific and memory-centric design; niches that plug into a hyperscaler's custom-silicon programme are the ones that get funded and acquired.

For Ecosystem Partners

The buyer-becomes-builder trend reshapes demand for EDA, packaging and networking; investors should track who supplies the picks and shovels as more operators design their own chips.

Read more 1 2 3

INVESTMENT & MARKET / SUPPLY CHAIN

Shortages & Inventory Dynamics · Long-Term Supply Agreements

The memory supercycle hardens: Micron locks in $100B as buyers brace for a multi-year shortage

Memory has stopped behaving like a commodity, and the June numbers made the shift explicit. Micron disclosed sixteen strategic customer agreements, fourteen of them carrying roughly $100 billion in minimum contracted revenue through 2030, alongside about $22 billion in cash deposits and commitments, the clearest sign yet that DRAM and NAND are being bought on long-term, take-or-pay terms rather than on the spot market. Its chief executive was blunt that supply shortages will take considerable time to ease and that the company has no clear line of sight on when supply catches up with demand, even as it expects gradual improvement in 2028.

The scarcity is reshaping the supply base in three directions at once. An industry forecast puts 300mm memory equipment investment above $50 billion in 2026 as makers race to add capacity. Downstream, module makers are diversifying sourcing: Chinese brands are increasingly designing in homegrown CXMT and YMTC DDR5, with some global PC and peripheral makers already adopting China-produced chips, and one executive argued that state-guided local DRAM and SSD supply now gives Chinese module makers an edge while the market leaders chase AI margins. Even foundries are entering the space, with TSMC reportedly partnering with Winbond to supply DRAM wafers rather than relying solely on the big three.

Taken together, the picture is a structural, multi-year tightening in which secure memory supply, and control over who makes it, has become a strategic contest, not a purchasing footnote.

What This Means For You

For Startups

Hardware teams should secure memory allocation early and treat controllers, compression and memory-optimisation IP as opportunities rather than afterthoughts.

For Ecosystem Partners

The shift to long-term contracts and diversified sourcing changes memory-market economics; investors should watch capacity build-outs and the rise of alternative domestic suppliers.

Read more 1 2 3 4 5

TECHNOLOGY DIRECTION / INNOVATION

Process Nodes & Scaling · Architecture Shifts

The angstrom era opens: IBM's sub-1nm nanostack and the 300mm leap for 2D transistors

Chipmakers are reaching the limit of making transistors smaller in the traditional way. They are now using 3D stacking and new materials to improve chip performance, IBM is changing how transistors are arranged, while Imec, ASML and TSMC are changing what transistors are made from.

IBM demonstrated the first sub-1 nm test chip at 0.7 nm (7 angstrom) using vertically stacked transistors across two bonded wafers. Compared with its 2 nm technology, it promises 50% higher performance, 70% better energy efficiency, nearly 100 billion transistors and 40% higher SRAM density. Commercial production may take approximately five years.

Imec, ASML and TSMC demonstrated 2D-material transistors on a standard 300-mm wafer at a 50-nm pitch, with 94% functioning successfully. They used MoS_2 for n-type and WS_2/WSe_2 for p-type transistors. It shows that 2D-material transistors can potentially be manufactured on standard 300-mm production lines, moving them closer to commercial use. This could enable smaller, faster and more energy-efficient chips when conventional silicon scaling reaches its limit, although mass production is still years away.

What This Means For You

For Startups

Design and materials teams should track nanostack and 2D-material integration as long-horizon shifts, and focus near-term efforts on packaging and heterogeneous integration where entry costs are lower.

For Ecosystem Partners

Angstrom-era scaling deepens reliance on advanced lithography, bonding and metrology; investors should look to the tool and materials layers that enable 3D and 2D-material devices.

Read more 1 2 3

TECHNOLOGY DIRECTION

Power & Energy Systems · New Materials & Substrates

SiC scales up for the AI rack: Infineon's data-centre power push and China's SICC gains on Wolfspeed

Silicon Carbide is a material used to make power-management chips. Unlike AI processors that perform calculations, SiC chips control and convert electricity supplied to servers. Compared with traditional silicon, SiC can handle higher voltage and temperature with less energy loss.

Infineon: Expanded its SiC power-switch portfolio and introduced a 24-kW SiC-based backup-power design for AI data centres. It also supplied GaN components for a solar-power optimiser.

SICC: Rapidly increased the production of SiC substrate wafers and is gaining on Wolfspeed.

Wolfspeed: Made no new announcement here; it is the established US SiC leader against which SICC is being compared.

Infineon makes SiC power technology, while SICC and Wolfspeed supply the underlying SiC material.

What This Means For You

For Startups

Power-IC and module teams should benchmark against these data-centre SiC references, and substrate-focused ventures should note how fast new entrants are taking share from incumbents.

For Ecosystem Partners

Value in wide-bandgap is spreading upstream to substrates and downstream to rack-level power systems; investors should watch the contested SiC materials base as demand shifts to AI.

Read more 1 2 3 4

TECHNOLOGY DIRECTION

RF & Imaging Silicon · On-Device AI Storage · Design Tools

Silicon for the edge and the design bench: Infineon's imaging radar, Samsung UFS 5.0 and new EDA tools

Edge technologies and chip-design tools advance

Infineon began mass-producing what it describes as the industry's first 8-transmit/8-receive automotive imaging-radar chip, enabling higher-resolution sensing with fewer modules. Samsung introduced UFS 5.0 storage, delivering up to 10.8 GB/s, more than twice the speed of UFS 4.1,to support on-device AI. Separately, Synopsys launched tools that jointly assess thermal, electromagnetic and mechanical effects, while Keysight and WIN Semiconductors partnered to reduce high-frequency RF-chip design risks.

Edge devices are gaining stronger AI and sensing capabilities, while advanced design tools are improving the chances of chips working correctly on the first manufacturing attempt.

What This Means For You

For Startups

RF, radar and edge-AI teams should track these reference parts and verification tools, since access to better signoff and measurement shortens the path from prototype to first-silicon success.

For Ecosystem Partners

Design-enablement and edge-sensing silicon are quietly compounding; investors should note how multiphysics EDA and RF measurement partnerships de-risk advanced designs.

Read more 1 2 3 4

TECHNOLOGY DIRECTION / INNOVATION

New Materials & Substrates · Emerging Devices

New materials stake their claim: rare-earth-free zinc oxide light and China's diamond supply chain

New semiconductor materials target sensing, power and supply-chain independence

A Japanese university-led team demonstrated a rare-earth-free, sodium-doped zinc oxide material that emits light under mechanical pressure, even from a light fingertip touch. Zinc oxide is a semiconductor, but this material is not intended for processors or memory chips. It could function as a sensing or light-emitting layer in pressure sensors, structural-damage monitoring, wearables and displays. Removing rare-earth elements could reduce costs, environmental impact and supply-chain dependence.

Separately, China launched what is described as its first end-to-end diamond-semiconductor supply-chain project in Zhengzhou. Synthetic diamond's excellent heat dissipation and high-voltage tolerance could support future high-power and high-frequency electronics beyond silicon carbide and gallium nitride.

Both developments explore new materials beyond conventional silicon while reducing dependence on constrained or foreign-controlled inputs. However, both remain long-term technologies rather than market-ready products.

What This Means For You

For Startups

Use touch-emissive materials and diamond electronics to spot future product ideas and defensible IP. But for your immediate product roadmap, stick to materials and processes you can reliably manufacture today.

For Ecosystem Partners

Materials sovereignty is becoming a competitive axis; investors should track which regions build end-to-end supply chains for next-generation and ultra-wide-bandgap materials.

Read more 1 2

POLICY & GEOPOLITICS

Industrial Policy & State Subsidies · Sovereign Capacity

The trillion-dollar policy wave: South Korea, Japan and India's ISM 2.0 are investing heavily to build their own semiconductor industries

South Korea

Announced an 800 trillion won (about USD 520 billion) public-private semiconductor plan. Samsung and SK Hynix will each build 2 new fabrication plants, focused on AI-related high-bandwidth memory and HBM packaging. The amount is roughly 10 times the direct subsidies under the US CHIPS Act. Faster approvals may allow plants to begin operating by the mid-2030s.

Japan

Introduced a JPY 101.6 trillion AI and semiconductor programme within its larger JPY 370 trillion (about USD 2.3 trillion) economic-growth roadmap through 2040. Around JPY 68 trillion is intended for semiconductors. Japan wants domestic chip sales to increase fivefold to JPY 40 trillion.

India's Semiconductor Push Expands: From ISM 1.0 to ISM 2.0

ISM 1.0 brought semiconductor projects to India; ISM 2.0 aims to build the domestic supply chain around them. Announced in the Union Budget for FY 2026–27 and approved by the Union Cabinet with an outlay of **₹1.27 lakh crore,** the six-year programme expands support across the wider semiconductor ecosystem.

1. The Foundation: ISM 1.0

Launched in December 2021 with an outlay of ₹76,000 crore, ISM 1.0 supported semiconductor and display fabs, compound semiconductor and ATMP/OSAT facilities, and domestic chip design. Under the programme, **12 semiconductor manufacturing units were approved, representing a cumulative investment of over ₹1.64 lakh crore.** It established India's initial manufacturing and design base, with support largely centred on individual facilities and design projects.

2. The Evolution to ISM 2.0

Building on ISM 1.0, ISM 2.0 adopts an ecosystem-wide approach covering both semiconductor projects and the upstream capabilities needed to sustain them. This expansion reflects the structure of the semiconductor industry, which depends on an extensive network of equipment manufacturers, material suppliers, chemical and industrial-gas producers, packaging companies, research institutions and specialised service providers.

The differences between the two phases

Pillar	Approach under ISM 1.0	Emphasis under ISM 2.0
Domestic IP and chip design	The Design Linked Incentive supported semiconductor design and access to EDA tools	Greater emphasis on developing domestic IP, chips and systems across compute, memory, power, networking, RF and sensor technologies
Machines and materials	No separate incentive category for semiconductor equipment and material suppliers	Incentives extended to the manufacturing and R&D of semiconductor equipment and the production of materials, specialty chemicals and gases
Setting up more fabs	Provided 50% support for silicon and display fabs based on project cost and for compound and discrete semiconductor fabs based on capital expenditure	CMOS-based silicon fabs will receive 40% of capital expenditure, while compound semiconductor, discrete component and display fabs will receive 35%, on a pari-passu basis
Strengthening ATMP/OSAT	ATMP/OSAT facilities received support equivalent to 50% of capital expenditure	Support differentiated by technology: 35% of capital expenditure for advanced packaging and 25% for conventional packaging, on a pari-passu basis
Research and development	R&D, skill development and training were supporting provisions under the earlier schemes	R&D becomes a distinct pillar, focusing on advanced process nodes and technologies through collaboration with research centres in India and overseas
Talent development	Training focused primarily on chip design through universities and access to EDA tools	Building on 315 participating universities and approximately 68,000 trained students, the programme will expand training across fabrication, packaging, clean-room operations and fab construction

ISM 2.0 represents a shift from facility-led support towards ecosystem-wide development. Its potential impact lies in attracting investment across the semiconductor supply chain, developing domestic suppliers of critical inputs, strengthening advanced packaging and R&D capabilities, and creating specialised talent, If implemented at scale, this wider coverage could increase domestic value addition, reduce dependence on imported inputs and improve India's resilience across the semiconductor value chain.

What This Means For You

For Startups

Design and materials teams should map their roadmaps to ISM 2.0's incentive categories, and watch Korea's and Japan's build-outs for supply and partnership openings.

For Ecosystem Partners

Trillion-dollar state commitments are redrawing where capacity lands; investors should factor sovereign-capacity policy into long-horizon location and supply-risk decisions.

Read more 1 2 3 4 5 6 7

UPCOMING SEMICONDUCTOR EVENTS

August 2026

Global Events

August 01-03 | International Symposium on Integrated Circuit Design and Integrated Systems (ICDIS)

Universidade de Aveiro | China

August 04 | Multiphysics Modeling of Semiconductors, Part 3: Surface Processing

COMSOL Multiphysics Pvt Ltd | Online

August 04-06 | FMS: Future of Memory and Storage

Terrapinn | USA

August 05 | AI Techniques in Semiconductor Manufacturing

SEMI | USA

August 10-11 | International Conference on Solid State Electronics and Semiconductor Physics (ICSSESP-26)

ASPHER, ISER, IIRD Global & Research Foundation. | Denmark

August 16-21 | The International Conference on the Physics of Semiconductors

International Union of Pure and Appplied Physics | Japan

August 17-20 | International Conference on Amorphous and Nano-crystalline Semiconductors (ICANS 31)

Wuhan University | China

August 17-20 | Inside the Fab: Intro to Semiconductor Manufacturing (Asia/EU)

SEMI | Singapore

August 18 | Understanding Semiconductor Technology and Business

SEMI Global | USA

August 19-21 | IEEE Hot Interconnects Symposium 2026

IEEE Computer Society | Virtual

August 21-22 | Overview of Semiconductor Manufacturing (Americas)

SEMI | USA

August 23-25 | Hot Chips: A Symposium on High-Performance Processors

IEEE (TCMM) and ACM SIGARCH | USA

August 23-27 | SPIE Optics + Photonics

SPIE | USA

August 24-25 | ICSST 2026 (International Conference on Semiconductor Science and Technology)

World Academy of Science, Engineering and Technology | Malaysia

August 24-28 | SBC/SBMicro/IEEE Symposium on Integrated Circuits and Systems Design (SBCCI)

University of Sao Paulo, IEEE CEDA | Brazil

August 24-25 | Plasma Etching, ALE, & RIE (Americas/EU)

SEMI | USA

August 25-27 | 21st Canadian Semiconductor Science and Technology Conference

University of Ottawa | Canada

August 26 | TechWorks: Semiconductors to Systems Summit

Tech Works | London, UK

August 26 | Semiconductor Awareness Days

SSIA | Singapore

August 26 | FEMC#30: High Throughput Material Development for Extreme Environment Printed Electronics

SEMI | USA

August 26-27 | International Semiconductor Executive Summits Korea

ISIG | South Korea

August 26-28 | Vietnam International Exhibition of Semiconductors, Optoelectronics and Smart Technologies (VISOTECH)

Camel Trade Exhibition and Promotion Events Company Limited | Vietnam

August 26-28 | Advanced Semiconductor Packaging & Chiplet Show (ASPS)

J. Expo Limited | South Korea

August 26-28 | World Summit and Expo on Semiconductors, Optoelectronics, and Nanostructure (SEMICON)

Scientific Summits | South Korea

August 26-28 | PCIM Asia Shenzhen 2026

Messe Frankfurt (HK) Ltd | China

August 27 | Semiconductor-MedTech Ecosystem Summit

SEMI | USA

August 28-30 | International Symposium on Advanced Semiconductor Devices and Integration Technology (ASDIT)

AEIC Academic Exchange Information Centre | China

Aug 31-Sep 02 | CSEAC 2026 (China Semiconductor Equipment & Core Components Expo)

CEPEIA | China

Indian Events

August 01-02 | Digital India RISC-V Symposium 2026

IIT Madras | Chennai

August 03-05 | Bengaluru India Nano

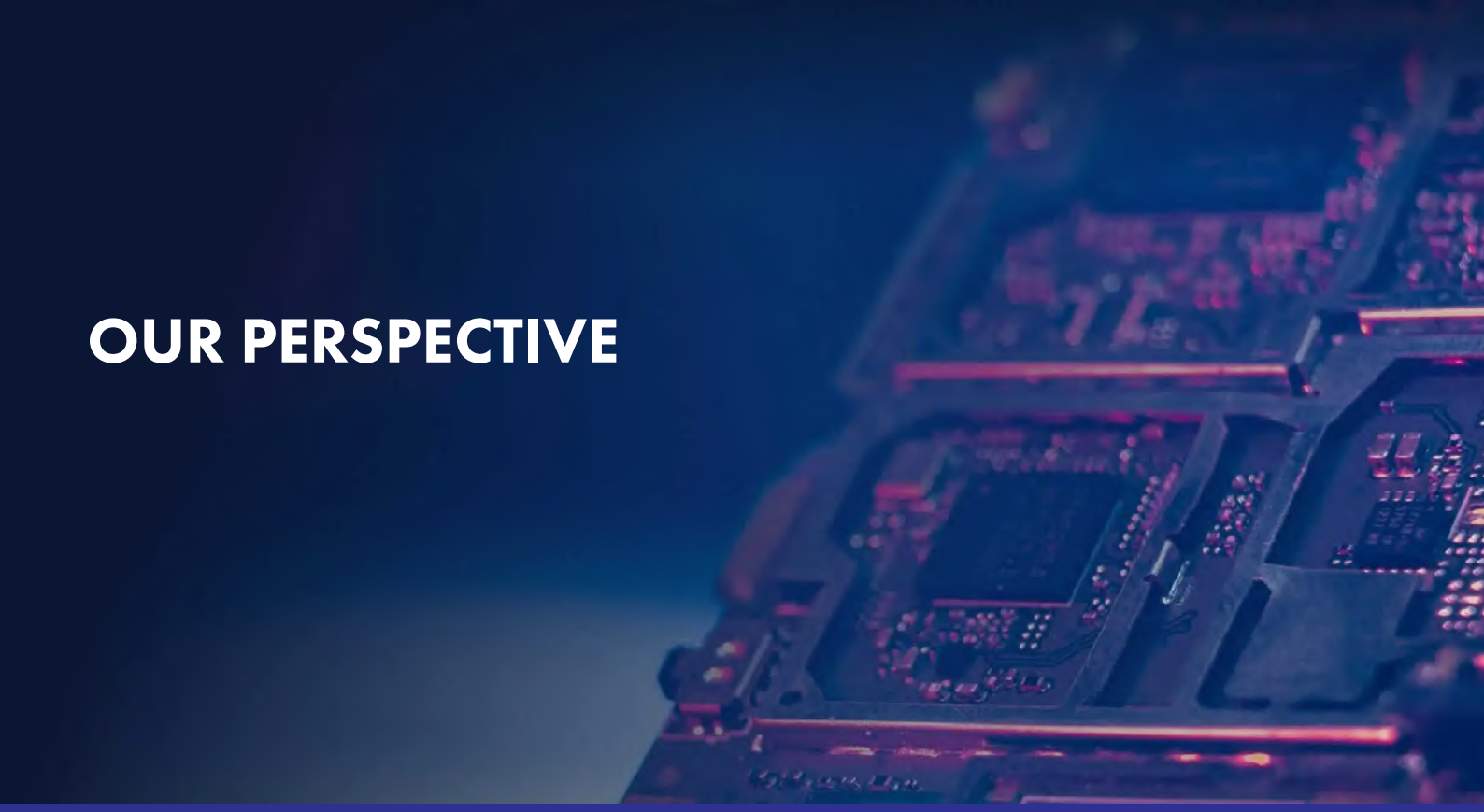
Department of Science & Technology, Govt. of Karnataka, and JNCASR | Bengaluru

August 07 | SFAL Day 2026

Semiconductor Future Accelerator Lab Foundation (SFAL) | Bengaluru

August 12 | CadenceLIVE India 2026

Cadence Design Systems | Bengaluru



OUR PERSPECTIVE

Together, these developments show that the semiconductor industry is expanding beyond chip fabrication into memory, advanced materials, power electronics, chip design, packaging, testing and supply-chain control. AI is increasing demand for memory, efficient data-centre power systems and faster edge devices, while technologies such as 3D stacking and 2D materials are changing how future chips will improve. Government investments and competition in SiC, diamond and other critical materials also highlight the growing importance of domestic capabilities.

For SFAL ecosystem, the strongest near-term opportunities are in chip design, EDA and verification, edge AI, power electronics, advanced packaging, testing and semiconductor materials. Experimental technologies such as sub-1-nm chips, 2D transistors, diamond semiconductors and rare-earth-free zinc oxide should remain on the long-term watchlist. Overall, India should build capabilities across the wider semiconductor value chain rather than focusing only on expensive fabrication plants.

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