

Future Semisphere

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Technology



Investment



Supply Chain



Policy



Innovation





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TECHNOLOGY DIRECTION / INNOVATION

GaN & Compound Semiconductors · Product Launches & Specs

GaN Beyond 2,200V: Power Integrations and Kubos Push the Voltage and Light Frontier

Power Integrations has demonstrated a GaN device operating at 2,200V. The demonstration shows that GaN could potentially be used in applications such as grid-tie inverters, industrial motor drives and traction systems, areas where silicon carbide (SiC) is commonly considered. The 2,200V device is still a technology demonstration rather than a commercial product, but it shows how far GaN technology is being pushed beyond its current production range.

Kubos, UK-based startup has raised USD 2.1 million in seed funding to develop cubic-phase GaN microLEDs for optical interconnects. The company is targeting short-distance optical links within AI computing clusters, where optical connections could help move large volumes of data between chips.

The two developments address very different applications, but they highlight the same trend, GaN is moving beyond its established use in consumer power chargers. The material is now being explored for higher-voltage power conversion as well as next-generation optical data links.

What This Means For You

For Startups



Power semiconductor startups can assess whether higher-voltage GaN could open opportunities in industrial, grid and traction applications. Startups working on optical interconnects can also track GaN-based microLED developments as demand for faster data movement in AI computing grows.

For Ecosystem Partners



Equipment and materials suppliers can watch for emerging requirements as GaN moves into higher-voltage applications and new optical technologies. Investors and industry partners can also track funding and commercial developments in GaN across power electronics and photonics.

[Read more 1 2](#)

TECHNOLOGY DIRECTION

Architecture Shifts & Compute Paradigm · Sensors, MEMS & Photonic Sensing

Memory and Light:

Samsung's 3D Memory Approach Meets the Growing Need for Optical Interconnects

Two developments highlight the same challenge in AI infrastructure. Chips are computing faster, but moving data fast enough is becoming harder.

Samsung unveiled its next-generation 3D memory approach, combining ZHBM (Zero-Height HBM) with V10 BV-NAND. ZHBM places memory directly on the logic die, shortening the distance data travels and helping reduce energy use.

Meanwhile, silicon photonics and optical interconnects are gaining importance as AI data centres scale. Copper connections face bandwidth and power limits across larger GPU clusters, while optical links can move more data over longer distances with lower power requirements.

The two approaches address different parts of the same problem, Samsung is moving data faster within the chip package, while photonics helps move it efficiently between chips and systems. Together, they show that memory and connectivity are becoming as important as computing power in scaling AI infrastructure.

What This Means For You



For Startups

AI chip startups need to consider memory bandwidth, power efficiency and data movement alongside compute performance. Photonics startups can also benefit from the growing need for high-speed AI connectivity.



For Ecosystem Partners

The growing US-China focus on photonics makes silicon photonics supply chains strategically important. Government and investment stakeholders should view photonics as an important part of AI infrastructure.

[Read more 1 2](#)

INVESTMENT & MARKET

VC, Private Equity & IPOs · M&A, Joint Ventures & Consortia

Photonics Gets Serious:

Olix's \$312M Raise and Nokia's InP Fab Bet Signal a Structural Shift

Photonics is moving closer to commercial AI and data-centre applications, with investment growing across both chip architectures and component manufacturing.

Olix, UK startup raised \$312 million to develop a photonic AI chip that aims to reduce the need for high-bandwidth memory (HBM). Its approach uses light to move data within the chip instead of electrons, which could help reduce latency and improve energy efficiency for AI inference.

Nokia announced plans to acquire NXP's semiconductor fabrication facility in Chandler, Arizona, and convert it for indium phosphide (InP) production for optical communications.

What This Means For You

For Startups



Startups working on photonic integration, optical interconnects and InP-based devices are entering a market attracting significant investment. The Nokia deal also highlights the importance of reliable InP supply.

For Ecosystem Partners



The Olix funding shows growing institutional interest in photonics, while Nokia's InP move highlights the importance of strengthening the supply chain. Together, these developments give investors and industry stakeholders a clearer indication of the commercial potential of photonics.

[Read more 1 2](#)

INVESTMENT & MARKET

VC, Private Equity & IPOs · Startup & Ecosystem Funding

India's Semiconductor Funding Moment: Indian Startups Raise \$206M

India's semiconductor startup ecosystem is seeing stronger funding and institutional backing.

An industry report found that, Indian semiconductor startups have raised \$206 million since 2022, with funding increasing over the years. Design-focused companies account for most of the deals, while startups working on process technology, materials and equipment have received smaller but more specialised rounds.

The funding activity points to growing investor interest in India's semiconductor sector. However, funding remains more limited as companies move towards commercial production. Seed and Series A funding is available, but the funding needed to take a product from first silicon to production at commercial volumes remains a gap.

What This Means For You



For Startups

Funding is becoming more accessible, particularly for design-led semiconductor companies. Startups in process technology, materials and equipment may need to demonstrate clear commercial applications, customer interest and a credible path to scale to attract larger rounds.



For Ecosystem Partners

For Ecosystem Partners The funding trend strengthens the case for supporting semiconductor companies beyond seed and Series A stages. More support is needed to help startups bridge the gap between early product development and commercial-scale production.

[Read more 1](#)

INVESTMENT & MARKET / POLICY & GEOPOLITICS

Fab & Capacity Investment · India Semiconductor Policy & Incentives

Customers, Capacity, and the Demand Gap: L&T's OSAT Shift, India's Chip Design Reality, and Global Fab Bets

Three developments highlight key semiconductor challenges. These include building capacity, finding customers, and securing supply.

L&T Semiconductor plans to move some OSAT work from overseas to India, supported by the Semicon 2.0 incentive framework. The move reflects growing confidence in India's packaging and testing capabilities.

For Indian chip design startups, building a working chip is only the first step. Some have completed tape-outs and demonstrated working silicon but are still struggling to secure paying customers and volume orders.

Globally, companies are investing to secure future chip capacity. Tesla and SpaceX announced a \$16.8 billion investment in a new Texas chip factory, while Sony and TSMC committed \$6.3 billion to a joint venture for next-generation image sensors in Japan.

Together, these developments show that India is building semiconductor manufacturing capacity, Indian startups need customers to turn designs into businesses, and global companies are investing directly to secure future chip supply.

What This Means For You

For Startups



A successful tape-out is only one step towards building a semiconductor business. Startups need to develop customer relationships and demand alongside their chip development, particularly as large companies increasingly look for greater control over their chip supply.

For Ecosystem Partners



The Tesla–SpaceX and Sony–TSMC investments show that large technology users are also investing directly in semiconductor capacity. Indian stakeholders can watch whether companies in sectors such as automotive, telecom and defence move in a similar direction.

Read more [1](#) [2](#) [3](#) [4](#)

SUPPLY CHAIN

Raw Materials & Substrates Security · Shortages & Inventory Dynamics

WF6 Under Pressure:

How the Tungsten Hexafluoride Squeeze is Testing the AI Chip Supply Chain

Tungsten hexafluoride (WF6) is a specialised gas used to form tungsten contacts in advanced logic and memory chips. As AI chip production expands, WF6 is emerging as a potential supply-chain bottleneck.

Demand is rising as 7nm-and-below wafer production increases, but supply is concentrated among a limited number of producers, mainly in Western Europe and Japan. New capacity can take 18–24 months to come online, while finding a direct substitute is difficult. Some feedstocks used to produce WF6 are also affected by export controls linked to US-China technology tensions.

In simple terms, AI chip production is growing faster than the supply of a specialised material needed to make these chips. This means even a small manufacturing input can become a bottleneck when chip production scales rapidly.

For companies planning a tape-out in the next 12 months, material availability could increasingly become part of foundry planning, alongside wafer capacity, cost, and lead times.

What This Means For You

For Startups



Fabless companies planning advanced-node tape-outs in 2026–27 should discuss WF6 and other critical process-gas availability with their foundry partners when planning production slots. Understanding these upstream constraints can help startups plan around potential delays.

For Ecosystem Partners

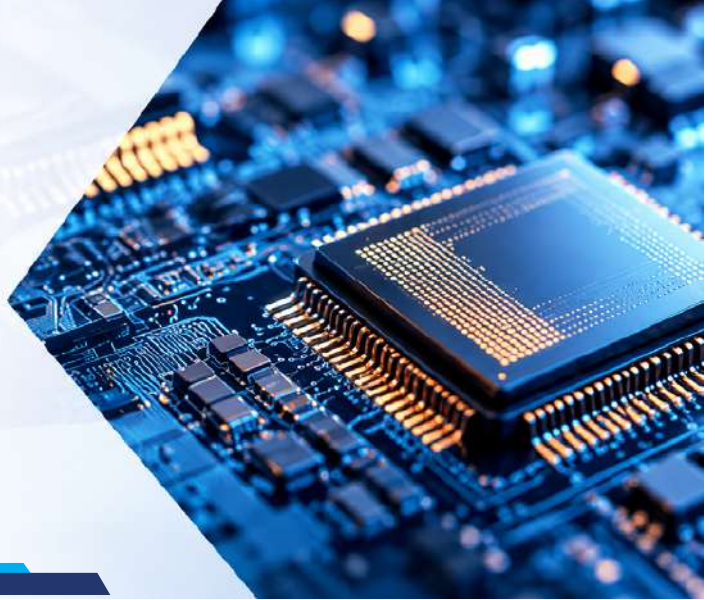


The WF6 situation highlights a type of critical-material constraint that can be overlooked in broader semiconductor supply-chain assessments. Investors and government stakeholders tracking supply-chain resilience should consider specialty process gases alongside more visible areas such as substrates and advanced packaging materials.

[Read more 1](#)

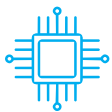
Feedback's PoV on Semicon 2.0

Semicon 2.0: From Proving the Concept to Building the Ecosystem



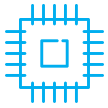
Feedback's view:

Semicon 2.0 is the most consequential shift in India's semiconductor policy since 2021 — not because of its size, but because of where it points. The first mission asked whether India could build and operate semiconductor plants; with twelve approved units, over ₹1,64,000 crore of committed investment and commercial production underway at Micron, CG Semi and Kaynes, that question has been answered. Semicon 2.0 asks a harder one: can India supply the machines, materials, chemicals, gases, designs and engineers that those plants consume? The ₹1,27,500 crore programme notified on 31 August 2026 is correctly aimed at that question. Its success, however, will turn less on incentive rates than on demand aggregation, qualification pathways, and whether the design pillar's new financing instruments are made workable for globally structured companies.



What Semicon 2.0 Changes

The programme is organised around six pillars and ten categories — design, equipment and materials, fabrication, assembly and advanced packaging, research and development, and talent. Three structural changes matter. First, **scope has widened from chips to the chip supply chain**, with equipment, specialty chemicals, electronic-grade materials and industrial gases becoming incentivised categories in their own right, supported at 30% of project cost and reinforced by a production-linked incentive of up to 10% of domestically sourced bill-of-materials value from FY2028–29. Second, **headline capex support has been reduced** — silicon wafer fabs now receive 40% of eligible capex on a pari-passu basis, against a flat 50% under Semicon 1.0 and up to 75% once state top-ups were counted. We read this as reallocation rather than retreat: with proof-of-concept risk substantially retired, the marginal rupee now buys more by deepening the supply chain than by further de-risking a single fab. Third, and least discussed, the design pillar has moved from grants to capital as addressed below in section 2.



The Design Pillar: Where Semicon 2.0 Genuinely Departs

Attention has concentrated on the fab and packaging numbers, but in our assessment the design pillar is the programme's most significant innovation. It is structured in two categories. The **strategic category** supports semiconductor IP, chips, SoCs and modules of national importance and for critical infrastructure, with intellectual property co-owned with C-DAC. The **commercial category** supports domestic fabless companies, startups and MSMEs through design infrastructure and EDA tool access, milestone-linked seed funding of 50% of project cost or ₹15 crore (whichever is lower), equity co-investment, and royalty financing. Eligibility is confined to companies owned by Indian citizens or Overseas Citizens of India, incorporated and headquartered in India with substantive local presence.

What is new is the instrument, not the quantum

For the first time, an Indian industrial programme proposes to act as a co-investor rather than a grant-maker. The government will match private capital from seed through Series A, B and C on terms equivalent to those of the lead private investor, positioning itself as a financial investor without involvement in day-to-day management. For founders unwilling to dilute, royalty financing offers an upfront lump sum recovered as 5% of net product revenue, capped at 1.5 times the support extended; larger eligible companies may access either route. This is, in effect, a sovereign venture-capital and venture-debt function embedded in industrial policy — a materially different proposition from the design-linked incentive it replaces.

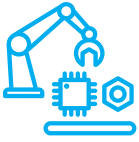
Why it matters

India holds roughly a fifth of the world's chip design engineers, yet the overwhelming majority work in the Indian centres of global fabless companies, with the resulting intellectual property held at parent headquarters. Of some 372 homegrown design startups, only about 11% have raised venture capital; total venture inflow since 2023 is approximately US\$161 million across 37 rounds — an average of US\$4.35 million, an order of magnitude below the cost of taping out a single complex SoC at an advanced node¹. The binding constraint has never been engineering capability. It has been patient risk capital, tool access and first customers. The earlier design-linked incentive addressed the easier problems creditably — 24 design projects approved and 105 startups and MSMEs given access to industry-standard EDA tools — but a grant capped in the low tens of crores cannot carry a company across a Series B funding cliff. An equity and royalty instrument can. Design is also the pillar with the highest potential return per rupee, because it requires no capital expenditure and no land, and because IP created in India is the only part of the value chain that cannot be relocated.

Many industry commentators have asked for the ownership and IP conditions need revisiting. Industry commentary has argued that C-DAC co-ownership in strategic silicon, combined with domestic lock-in, constrains cross-border licensing, clean spin-outs and mergers and acquisitions — precisely the exit paths that global venture investors underwrite.

Our own position is that sovereign control of strategic silicon is a legitimate and necessary objective, but that the strategic and commercial categories should be allowed to operate under different IP and ownership regimes. If they are not, the commercial category will inherit restrictions designed for the strategic one, and the pillar (Design) that asks least of the exchequer and returns the most per rupee committed will struggle hardest to attract private capital.

¹ India's share of the global chip design engineering workforce, the retention of resulting intellectual property at parent headquarters, the count of 372 homegrown design startups of which approximately 11% are venture-funded, and venture inflow of about US\$161 million across 37 rounds since 2023 (Tracxn data), are reported in 'Time to plug chip design gap as Semicon 2.0 seeks to boost startups', Business Standard, 9 September 2026.



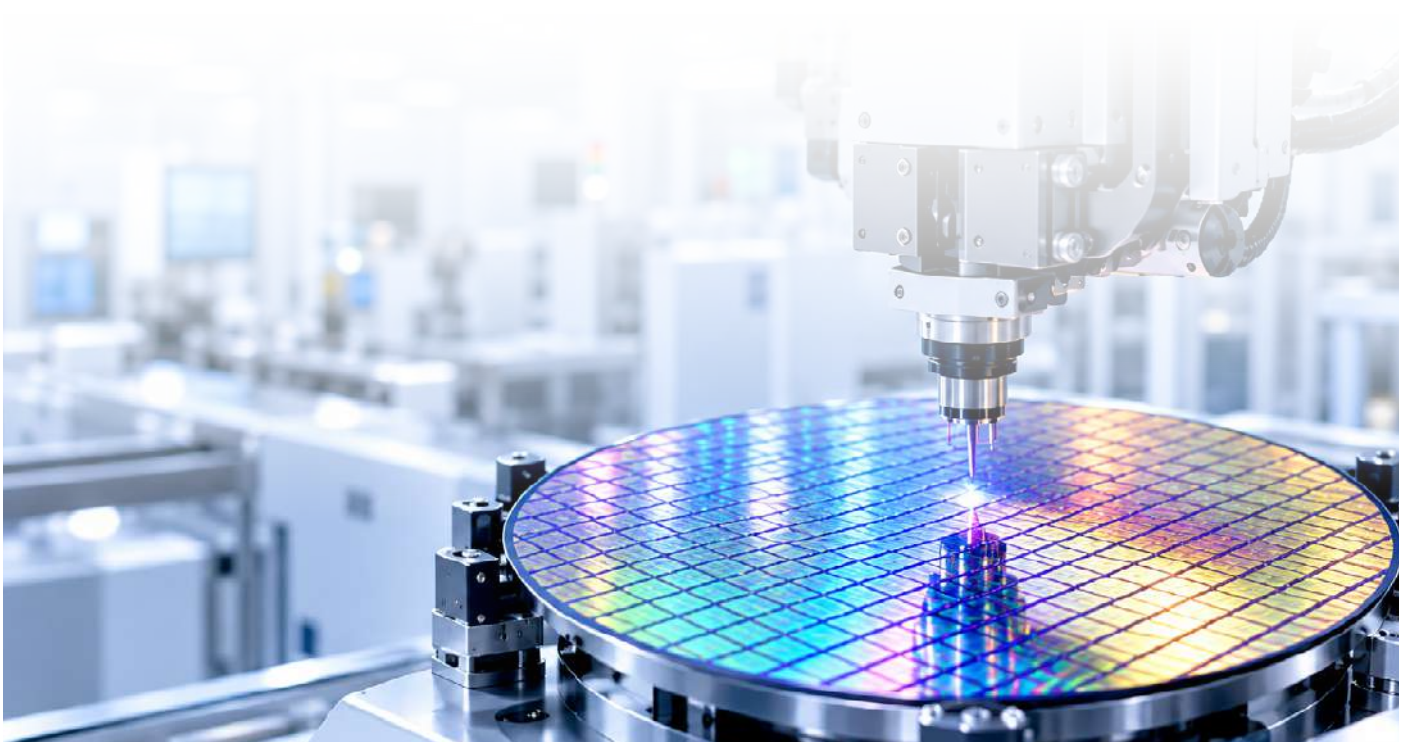
Manufacturing: Chips to Chips Supply chain focus

In the manufacturing sector, Semicon 2.0 exhibits greater differentiation than Semicon 1.0. Rather than addressing packaging support in a broad manner, **it distinguishes between advanced and legacy packaging, providing enhanced support for advanced technologies such as 2.5D/3D packaging, chiplets, and heterogeneous integration.** This distinction is significant because the global competitiveness of the semiconductor industry is increasingly shifting from mere node advancement to packaging and system-level integration. Furthermore, the inclusion of incentives for equipment, materials, chemicals, and gases addresses a notable deficiency in Semicon 1.0: the lack of a robust domestic upstream supply base for fabrication facilities.



The Measure of Success

Semicon 2.0 should not be judged by the number of approvals it generates. The meaningful metrics are the share of bill-of-materials value sourced domestically by India's fabs and OSATs, the count of Indian suppliers formally qualified into production lines, the engineer-hours logged on live tools rather than in classrooms, and — the one we would watch most closely — the number of Indian fabless companies that reach a funded Series B with a product in volume production. On each measure India begins from a low base, which is precisely why the widened scope is the right bet. The policy architecture is now substantially correct; the execution risk has shifted to guideline velocity, centre–state alignment, the willingness of established players to open their supply chains, and the terms on which the state proposes to sit on a startup's capitalisation table. Feedback Advisory would welcome engagement with stakeholders across industry, government and academia on any of these themes.



OUR PERSPECTIVE

This edition highlights how the semiconductor opportunity is expanding beyond chip design and fabrication into packaging, advanced memory, photonics and specialised materials. At the same time, growing AI-driven demand is putting pressure on the supply chains supporting advanced semiconductor production, from manufacturing capacity to critical process materials.

For the SFAL ecosystem, India's growing funding activity and the shift towards domestic OSAT show that the ecosystem is moving from early-stage capability building towards greater commercial participation. The continuing gap in paying customers, however, shows that building technical capability alone is not enough; startups also need pathways to customer adoption and scale.

Globally, investments in AI infrastructure, optical technologies and dedicated chip capacity are also changing where opportunities are emerging across the value chain. Startups and ecosystem partners that track both India's capacity build-out and these global technology and supply-chain shifts will be better positioned to identify where new opportunities are developing.



Future Semisphere

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